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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
|-----------------|-------------|----------------------|---------------------|------------------|

10/698,454

11/03/2003

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YUJ13002/EM

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EXAMINER

ABDIN, SHAHEDA A

ART UNIT

PAPER NUMBER

2629

MAIL DATE

DELIVERY MODE

09/21/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

| | | | |
|------------------------------|-------------------------------|-------------------------------|--|
| Office Action Summary | Application No. 10/698,454 | Applicant(s) YU, JIAN-SHEN | |
| | Examiner Shaheda A. Abdin | Art Unit 2629 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11/03/2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.
2. The disclosure is objected to because of the following informalities: In page 4 paragraph 10, in lines 1 – 2, "switch elements 220" recited. Numeral 220 is not contain in the drawing.
3. In page 4 paragraph 15, lines 7-8, " 'spare output leads 281 and 282" recited. There is no switch element 220 is contained in the drawing. . Numeral 282 is not contain in the drawing.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1- 2, 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US Patent No: 5555001) In view of Dacosta et al. (US Patent No: 6281891).

(1) Regarding claim 1:

Lee teaches repairing structure (repairing process) of an integrated driving circuit (IC) for flat panel displays (5), in cooperation with at least one driver chip (3 or 7, Fig. 1), comprising (see Fig. 3, column 3, lines 9-15):

a plurality of video signal lines (signal from video, RGB) connected to the driver chip for supplying video signals (see Fig. 1, column 3, lines 9-15);

a multiplexer unit (e.g. 8, 8',10, Fig. 3) connected to said plurality of video signal lines (D1-D64 lines) (note that sub circuit 8 - 8' are interpreted as a multiplexer which is included a demultiplexer 10, therefore, the driving circuit uses a multiplexing arrangement, see, column 1, lines 44-54, column 5, lines 30-48);

a plurality of data lines (Lv1-Lv6) connected to said multiplexer unit (86 e.g. 8, 8',10);

and a display area (5, illustrated in fig. 1) connected to said plurality of data lines (Lv1-Lv6 lines, see Fig. 3) so that at least one driving circuit (e.g. shift register illustrated in Fig. 1) outputs said video signals (D1-D64 lines) to said multiplexer unit (e.g. 8, 8',10,) through said video signal lines and then data signals are output to said display area through said multiplexer unit and said plurality of data signal lines (column 4, lines 11-54, column 5, lines 30-48).

plurality of spare input-leads (e.g. Lh1-Lh2) and a plurality of spare output-leads (Lh3-Lh6) for repairing the connection between said multiplexer unit (e.g. 8, 8',10) and said at least one driving circuit (7)lines 30-48, column 6, lines 23-39 and Fig. 3).

Note that Lee teaches spare input-leads and spare output-lead but and a multiplexer unit but Lee does not teach a multiplexer unit comprises at least one dummy portion.

However, Dacosta teaches a multiplexer (86) unit comprises at least one dummy

portion (lines in TAB 90, interpreted as dummy lines or dummy portion) (column 10, lines 57-67, column 11, lines 1-10, see Fig 4).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate a multiplexer with dummy portion as taught by DaCosta in to the display system of Lee so that a plurality of spare input leads and a plurality of spare output leads from a dummy portion of a multiplexer could be use for repairing the connection between the multiplexer unit and the at least driving circuit. In this configuration the system would provide a reliable data connection in display devices with less cost (DaCosta, column 5, lines 32-42).

(2) Regarding claim 2:

Lee teaches spare input leads (Lh1, Lh2) and spare output leads (Lh5, L6) cross (cross in point 26 for video data and cross in point 28 for data signal video signal lines (in put data D1-D64) and said data lines (internal data LV1-Lv64) respectively without any connection (with out any hardwire connection) there between (see fig. 3, lines, and column 4, lines 11-54).

(5) Regarding claim 5:

Lee teaches that at least one said output-lead (e.g.Lh3) is connected (e.g. connected in point 28) to at least one said data line (Lv1) when said multiplexer unit (e.g. 8, 8', 10, Fig. 3) fails to connect said at least one data line connected to said display area (panel 5, illustrated in Fig. 5) (column 6, lines 45-53, Fig. 3).

(6) Regarding claim 6:

Lee teaches at least one output-lead (Lh3) is connected (e.g. connected in point 28) to said at least one data line (Lv1) by laser repairing technology (column 5, lines 10-45, column 6, lines 44-53 and Fig. 3).

(7) Regarding claim 7:

Lee teaches said multiplexer unit (e.g. 8, 8', 10, Fig. 3) is further connected to at least one control signal line (e.g. $\phi_{1,0}$) to receive control signals output from said at least one control signal line (column 3, lines 50-67), and at least one said spare input-lead (Lh1) is capable of repairing (repairing at point 28) the connection between said at least one control signal line and said multiplexer unit (e.g. 8, 8', 10, Fig. 3) (note that the control signals are applied to the data driving circuits 2 . . . 4, and 6 to multiplexer unit, therefore, the repairing process (see fig. 3) is occurred between the connection (connection at point 28) of at least one control signal line and said multiplexer unit (column 3, lines 50-67, column 6, lines 23-40).

(8) Regarding claim 8:

Lee teaches said multiplexer unit (e.g. 8, 8', 10, Fig. 3) has input connecting lines including said spare input-leads (e.g. Lh1-Lh2), said video signal lines (D1-D64) and said at least one control signal line (e.g. $\phi_{1,0}$), the number of said input connecting lines (the number of input connection lines are interpreted as (Lh1-Lh2)+ (D1-D64)+ $\phi_{1,0}$) is more than that of said video signal lines (Lh1-Lh2) (note that the number of input connection lines are (Lh1-Lh2)+ (D1-D64)+ $\phi_{1,0}$ and which will be larger than the video signal lines (D1-D64) (also see, Fig. 3, column 3, lines 50-67).

6. Claims 3—4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Dacosta as applied to claim 1 above, and further in view of Nakazawa et al (US Patent No: 5268678).

(3) Regarding claim 3:

Lee teaches said spare input-leads (Lh1, Lh2) are used with the multiplexer unit (e.g. 8, 8', 10, Fig. 3) for driving circuit and video signal line. Note that both Lee and Dacosta do not teach the spare input-leads are used for connecting the video signal when failure occurred.

However, Nakazawa teaches spare input-leads (103a, 103b) for connecting (note at point 115a) the video signal line when failure (break down the system) occurs (column 14, lines 50-62, Fig. 8A).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate the input-lead for connecting the video signal line when failure occurs as taught by Nakazawa into the system of Lee as modified by Dacosta so that the spare input-leads can be used when the multiplexer unit fails to connect at least one of the video signal line connected to the at least one driving circuit, and at least one of the spare input-lead can be connected to the at least one video signal line. In this configuration the system would provide a reliable data connection in display devices with less noise (Nakazawa, column 6, lines 1-6).

(4) Regarding claim:

Lee et al teaches said at least one spare input-lead (Lh1) is connected to said at least one video signal line (D1) by laser repairing technology (column 5, lines 10-45, Fig. 3).

(4) Regarding claim:

Lee et al teaches said at least one spare input-lead (Lh1) Is connected to said at least one video signal line (D1) by laser repairing technology (column 5, lines 10-45, Fig. 3).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's discloser.

Edwards et al. (US 7123232 B1) discloses an active matrix array devices.

Castleberry et al. (US 4688896) discloses an information conversion devices with auxiliary address lines for enhancing Manufacturing yield.

Inquiry

8. Any inquiry concerning this communication should be directed to the examiner at (571) 270-1673 Monday- Friday 7:30 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen, can be reached at (571) 272-7772.

Information regarding the status on an application may be obtained from the Patent Application information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>.

Should you have questions on access to the Private PAIR system, contact the

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Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9799 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner of patents and trademarks

Washington, D.C. 20231


Or fax to:

(703)872-9314 (for Technology Center 2600 only)

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09/14/2007

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SUPERVISORY PATENT EXAMINER